Utmost IV Delivers Full Capability of RPI TFT Models

Introduction

Silvaco SmartSpice has been a de facto standard analog circuit simulator from the inception of the TFT (Thin Film Transistor) technology industry. The early introduction of SPICE compact models developed by Rensselaer Polytechnic Institute (RPI) for poly silicon (poly-Si) and amorphous silicon (a-Si) TFT devices made integrated circuit design possible. Silvaco Utmost III SPICE parameter extraction tool played a critical role by providing the TFT model parameters for circuit designers. Modeling engineers have accumulated expertise in the RPI TFT models, especially for the poly-Si TFT model. Despite this expertise, the rapid technology advancement in recent years started to demand productivity improvement for the task of modeling and better performance in model fitting. This application note shows how Silvaco Utmost IV hybrid optimizer, a combination of genetic algorithm and traditional Levenberg Marquardt optimizers, can ease both burdens of the TFT modeling engineers. Two examples of Utmost IV parameter optimizations using the RPI poly-Si and a-Si TFT models will be shown.

Sophistication in RPI TFT Models

There are two RPI TFT models in SmartSpice: the amorphous silicon (a-Si) Level 35, and the poly silicon (poly-Si) Level 36 TFT models. The numbers of the DC model parameters are twenty four and thirty one for the a-Si and the poly-Si TFT models, respectively. Both models can be said to be very compact from the point of the parameter numbers. However, their equations are quite complicated and non-linear, which means that model parameter extraction using the traditional approach of Levenberg Marquardt (L-M) method is not easy. The L-M method provides good model fitting to the target measurement data when the initial model parameters are relatively close to the final solution. The condition is problematic for the TFT modeling engineers. Little information for the initial model parameter values is obtained from the DC current voltage characteristics. The complicated non-linear equations would fail to reveal the potential capability unless good initial parameter values are obtained.

Utmost IV Hybrid Optimizer: A Combination of Two Optimization Algorithms

Utmost IV provides six optimization algorithms. Two out of six are called as the local optimization algorithm, and the rest are the global optimization algorithm. The local optimizers require reasonable initial parameter values, while the global optimizers don't. Any two algorithms could be combined to form a hybrid optimizer in Utmost IV. The hybrid of the global and the local optimization algorithms is suitable for the RPI TFT model parameter optimization. The global optimizer searches the vast parameter space to find the so-called global minimum area, then, the local optimizer can find the best possible solution without worrying about the local minimum.

The following two examples show both the RPI TFT model sophistication and the Utmost IV capability.

1. RPI Poly-Si TFT Model Parameter Extraction Example

The following N type TFT example shows Utmost IV hybrid optimizer capability in extracting RPI poly-Si TFT model parameters. The optimization algorithms used are first the genetic, and second, the Levenberg Marquardt algorithms. The genetic algorithm optimizer is expected to give reasonable initial parameter values for the L-M approach.

The overall optimization sequence is initiated with a step for Ids versus Vgs under several Vds voltages. The drain leakage current at the negative Vgs and the sub-threshold to the weak inversion current regions are to be used. The sub-threshold current region forms the foundation of the entire drain current. The negative Vgs drain leakage current has to be connected smoothly to the sub-threshold current. Several parameters of the RPI poly-Si TFT model have influence both on the sub-threshold and saturation current regions. The number of parameters used for the sub-threshold region is smaller than that used for the saturation. In other words, the parameter optimization for the sub-threshold current region is less flexible than for the saturation in terms of the parameter numbers. The objective is, to get reasonable values of the

common model parameters for the sub-threshold region. The subsequent steps of the saturation region should be based on these parameters.

1-1. Utmost IV RPI poly-Si TFT Model Optimization: Step 1

Figure 1 is the target (green) and the default model parameter simulation curves (red). Level 36 version 2 with ISUBMOD =1 was used. The target data which exhibit TFT characteristics are modified artificially from the measurement data.

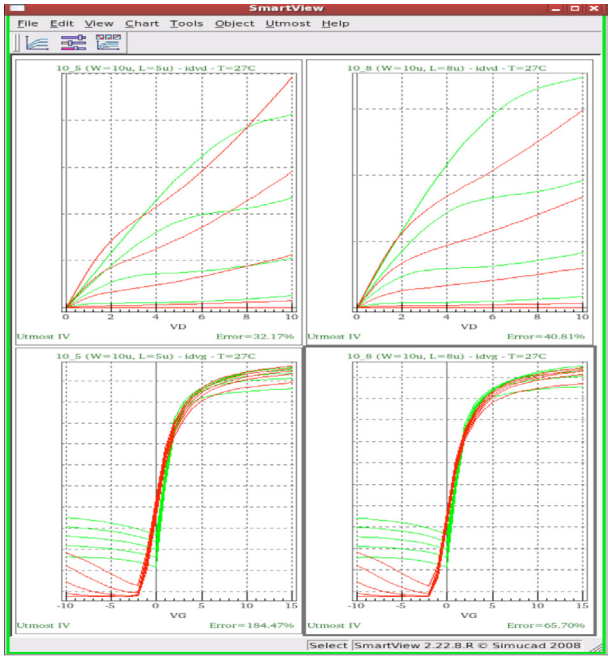

Figure 1: poly-Si TFT target data and default RPI poly-Si TFT model simulation curves in the green and red colors, respectively.

Figure 2 is a target region setup for the first optimization step in Utmost IV using the logarithmic scale data of Ids versus Vgs with Vds steps. The initial optimization step is designed to obtain the sub-threshold region and the leakage current at the negative Vgs region. Utmost IV optimization setup allows the multiple target selections for the same device data as shown in the red rectangles. The genetic algorithm searches the global parameter space to give the reasonable initial values. The Levenberg Marquardt method then tries to reduce the fit errors.

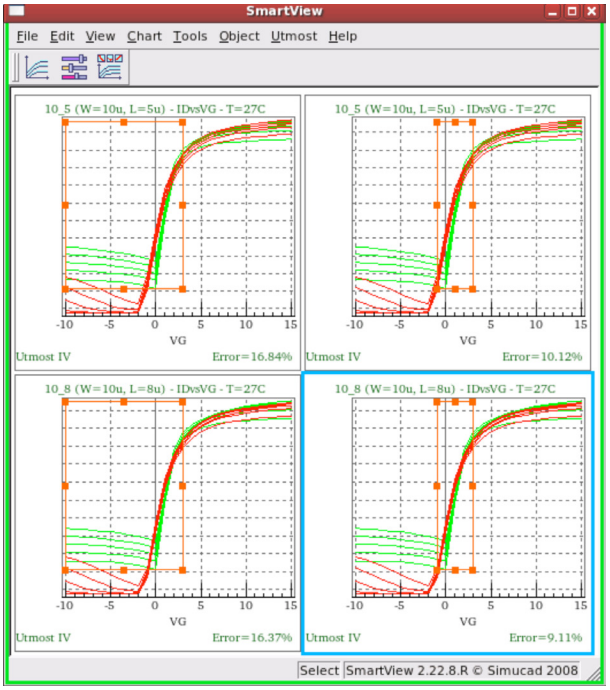

Figure 2: Utmost IV first optimization setup: both the sub-threshold and the negative Vgs regions are defined as the target.

Figure 3 shows a result of the first step. Although a stand-alone Levenberg Marquardt method might give a similar result, the hybrid with genetic algorithm is able to reduce the risk of unreasonable fitting using the default parameter values.

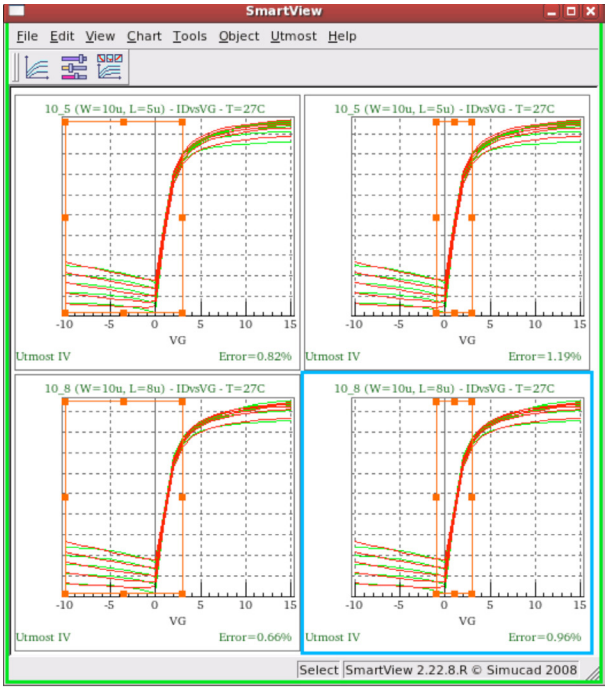

Figure 3: Utmost IV step 1 result of RPI poly-Si TFT model parameter optimization.

Figure 4 is an Utmost IV optimization project window to show an example of the optimization status. The initial fit error of 15.09 % was reduced to 5.72 %, then to 0.85 % by the hybrid optimizer.

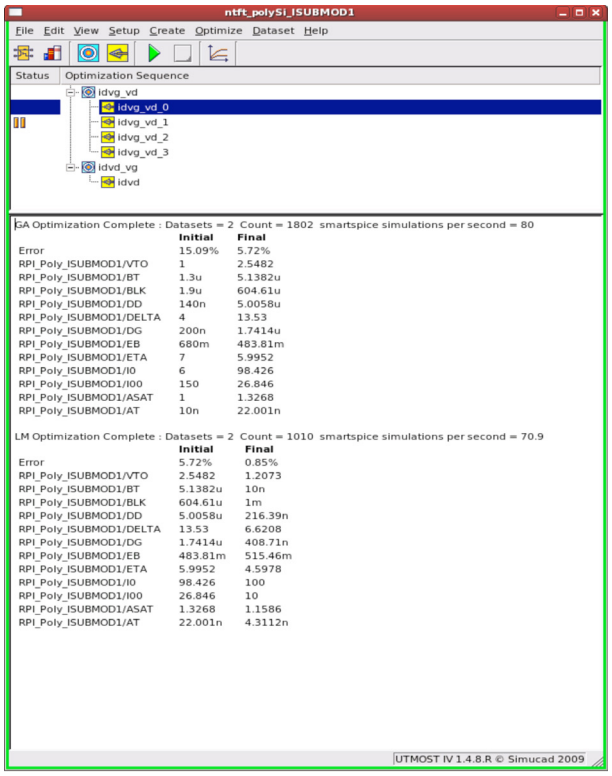

Figure 4: Utmost IV optimization status showing the hybrid optimizer.

1-2. Utmost IV RPI poly-Si TFT Model Optimization: Step 2

Figure 5 is a region setup of the second optimization step. Both the linear and the logarithmic scale data of Ids versus Vgs with several Vds are selected. The intention is to get a reasonable fit for the linear Ids current with less damage on the sub-threshold current region. Several parameters of RPI poly-Si TFT model have effects both on the sub-threshold and the linear/saturation current regions. The target minimum current value of the linear scale data is important as Utmost IV calculates the fit errors according to the Y axis scale. The logarithmic scale gives the looser error criteria than the linear scale does. Although both the logarithmic and the linear scale data are selected, the sub-threshold current region could lose the reasonable fit when the fit error reduction in the logarithmic scale data is much less than in the linear case. The Utmost IV target range of the minimum current for the linear scale data has to include the sub-threshold current values. Also, the sub-threshold target region of the logarithmic scale data has the larger optimization weight than the linear scale data range has.

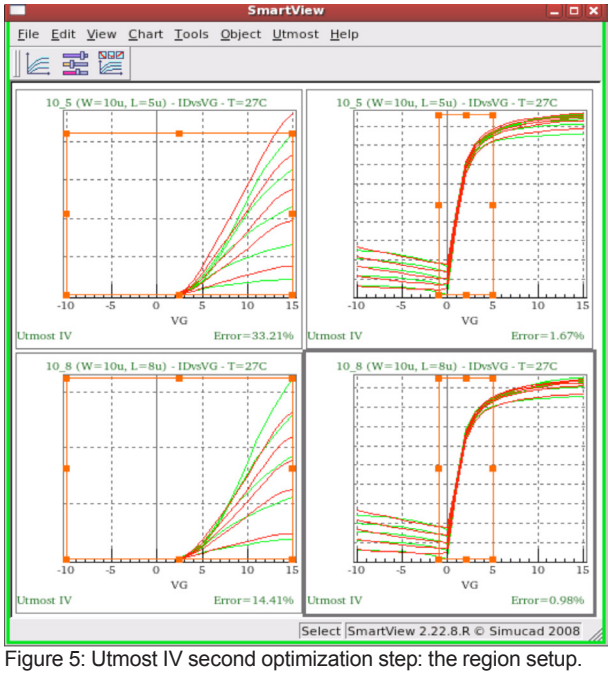

Figure 5: Utmost IV second optimization step: the region setup.

Figure 6 shows the result of the second optimization step. Although a small degradation in the sub-threshold region fitting is observed, reasonable fits for both the linear and the logarithmic scale data are obtained. Figure 7 is the optimization status to show another example of the hybrid optimizer. Almost all model parameters except for the leakage equation parameters are selected. This is a good example of using the genetic algorithm optimizer which allows the modeling engineer to roughly select the parameters.

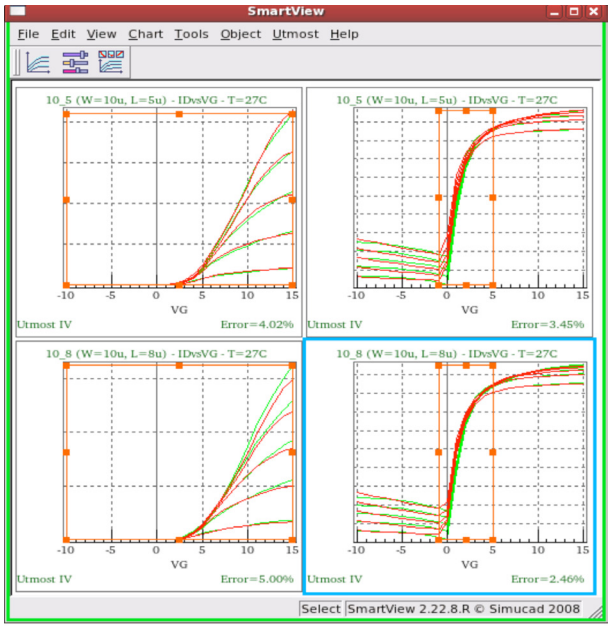

Figure 6: Utmost IV RPI poly-Si TFT model optimization, the second step result.

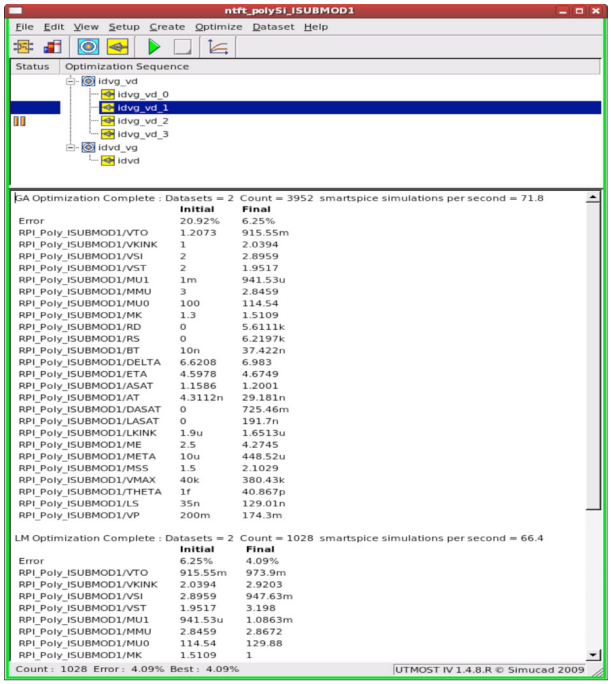

Figure 7: Utmost IV optimization status showing the hybrid optimizer.

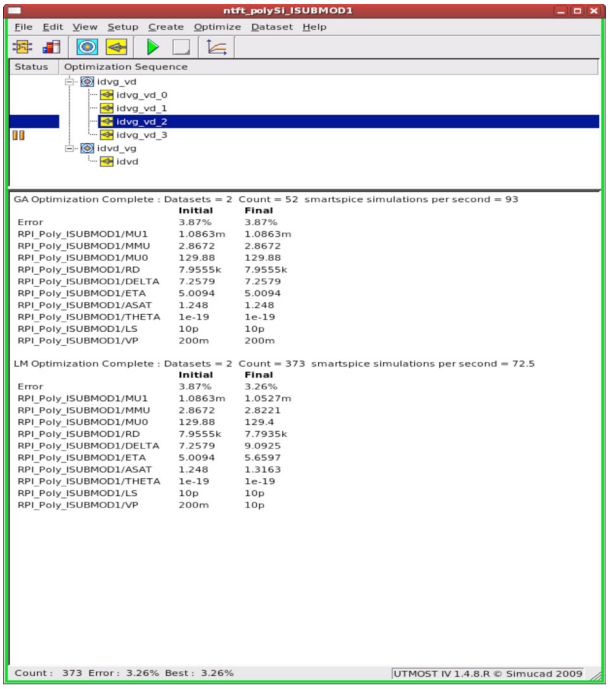

Figure 9: Utmost IV optimization status showing the less improvement.

1-3. Utmost IV RPI poly-Si TFT Model Optimization: Step 3

Figure 8 shows the third step of Utmost IV RPI poly-Si TFT model optimization, which is arbitrary. The intention is to ensure better values of the key model parameters. The number of target curves is reduced to the middle range of Vds steps. Figure 9 of the optimization status indicates that the second step is almost sufficient and that further large improvement would be difficult.

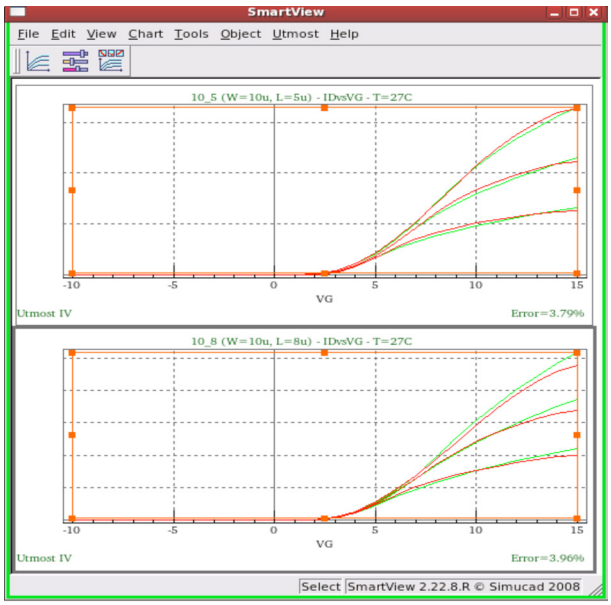

Figure 8: Utmost IV RPI poly-Si TFT optimization: the third step result.

1-4. Utmost IV RPI poly-Si TFT Model Optimization: Step 4

The final step is to use Ids versus Vds under several Vgs voltages. The previous steps using Ids versus Vgs cover the different aspects of Ids versus Vds in terms of the voltage setting. The model fitting before this step should give a reasonable result. Figure 10 shows Ids versus Vds curves right after the previous optimization steps. Even though no parameter optimization for the Ids versus Vds

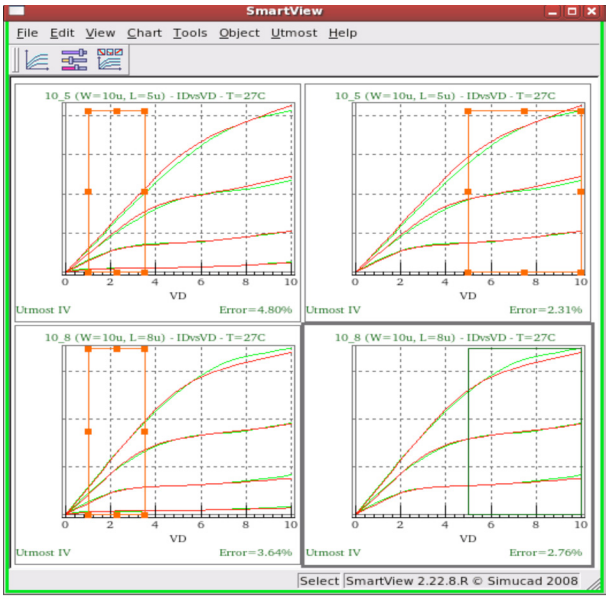

Figure 10: Utmost IV RPI poly-Si TFT model right after the Ids versus Vgs optimization.

was performed, the RPI poly-Si TFT model expresses the length scalable target well. The intention of this step is to improve the model further using the Levenberg Marquardt optimizer.

Figure 11 shows the fit error improvement for the Ids versus Vds curves. Although the improvement on Figure 12 isn't large, the Levenberg Marquardt optimization fitted the model in detail to the target curves.

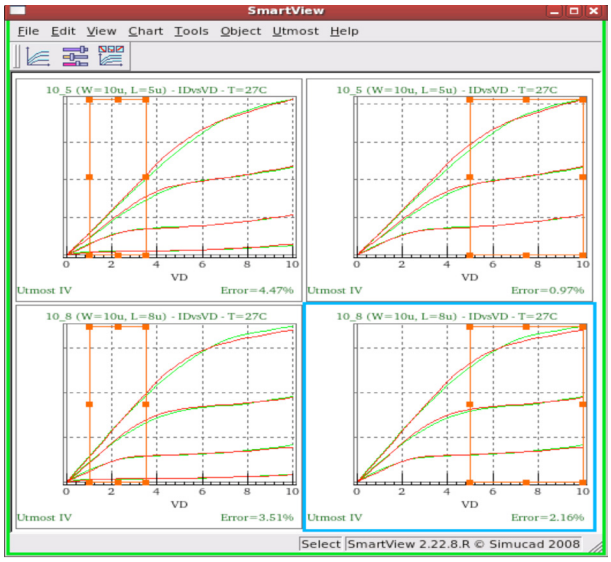

Figure 11: Utmost IV RPI poly-Si TFT model Ids versus Vds optimization.

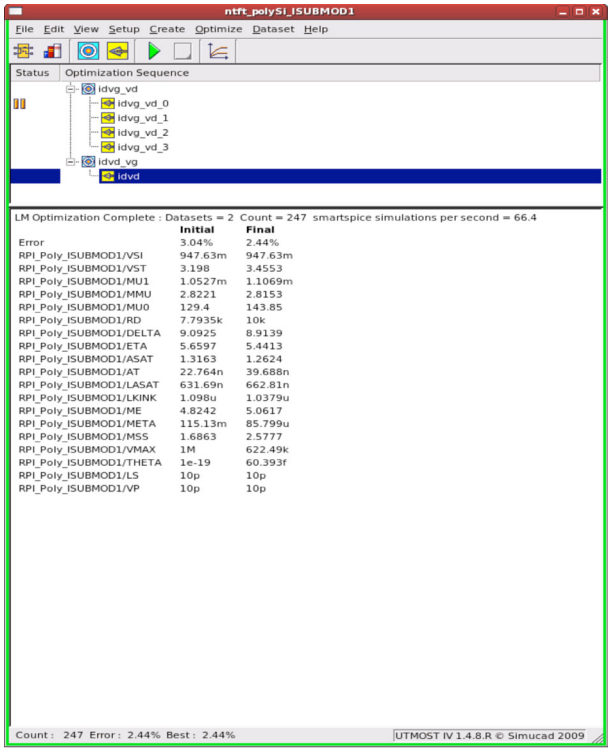

Figure 12: Utmost IV optimization status for the final step.

1-5. Utmost IV RPI poly-Si TFT Model Optimization: The Tuning

Figure 13 shows a good expression of the RPI poly-Si TFT model for the target characteristics. Readers may think whether the sub-threshold region could become better.

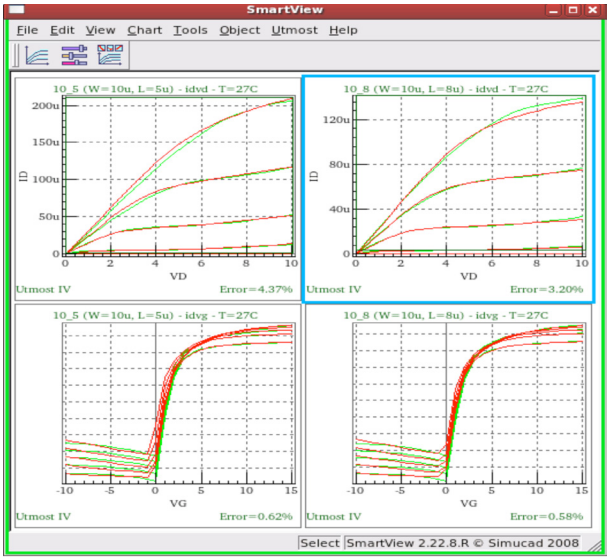

Figure 13: RPI poly-Si TFT model expresses both Ids versus Vds and Ids versus Vgs curves well.

The same Utmost IV optimization sequence could be run from the start as the continuous mode. Figure 14 is the result, after several iterations, of the same sequence. The sub-threshold region is clearly improved.

The fit errors of Ids versus Vds curves were 16.4 % and 7.9 % for the L = 5 um and 8 um devices, respectively.

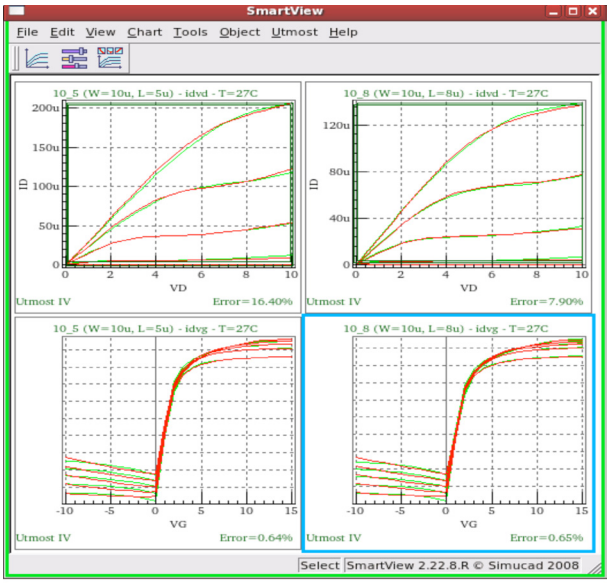

Figure 14: RPI poly-Si TFT model expresses both Ids versus Vds and Ids versus Vgs curves well. The sub-threshold region is improved compared to the figure 13 with no degradation of the saturation region current.

2. RPI amorphous-Si(a-Si) TFT Model Parameter extraction example

An example of RPI a-Si TFT model optimization is similar to the poly-Si TFT example. The target dataset was generated with Silvaco TCAD tools, the input file for which is based on the TCAD example of tftex05.in [1]. The parameter optimization flow for the RPI a-Si TFT model is almost the same as for the RPI poly-Si TFT model. The sub-threshold and the negative Vgs drain leakage current regions are optimized first, and the saturation current region is used with a constraint of keeping the sub-threshold region fit. Finally, the Ids versus Vds characteristics is used.

2-1. Utmost IV RPI a-Si TFT Model Parameter Optimization: Step 1

Figure 15 is the target data and the default RPI a-Si TFT Level-35 version 2 model simulation curves. The default parameters are apparently far away from the target. Utmost IV hybrid optimizer capability of the genetic algorithm and the Levenberg Marquardt method is challenged.

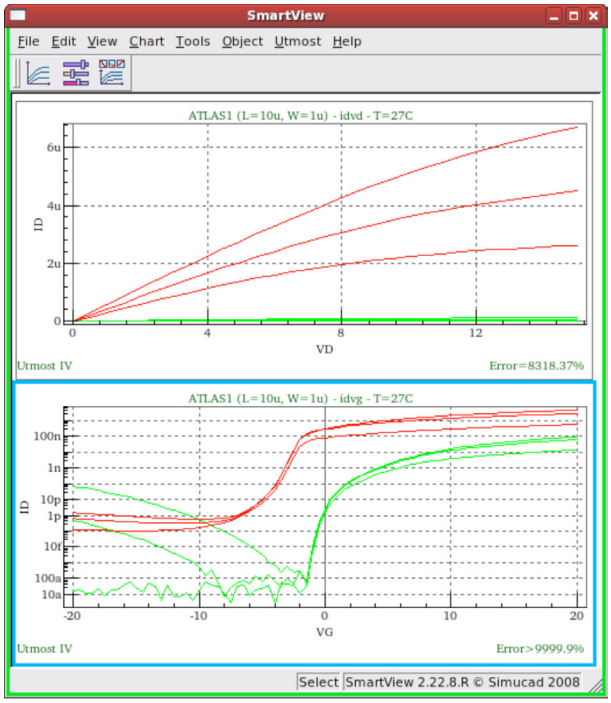

Figure 15: a-Si TFT target data and default RPI a-Si TFT model simulation curves as the green and the red colors, respectively.

Figure 16 shows the first step, the range setup of the optimization using Ids versus Vgs. The optimization target is specified in the linear scale data including the negative Vgs drain leakage current region. The logarithmic scale data is used to observe the optimization result, so that no optimization target is specified, which is indicated by the red rectangle out of the target data.

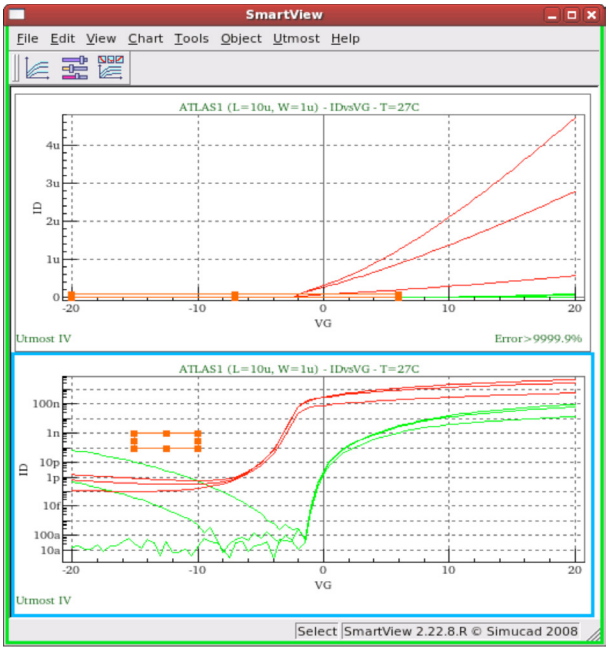

Figure 16: Utmost IV first optimization setup for a-Si TFT, both the sub-threshold and the negative Vgs regions are defined as the target. The logarithmic scale is used to observe the result. The rectangle box out of the target data indicates no parameter optimization is performed.

Figure 17 and Figure 18 show the optimization result and the optimizer status, respectively. Even though the initial simulation curves were far away from the target, Utmost IV hybrid optimizer was able to find the solution close to the target for the sub-threshold region. The negative Vgs region needs subsequent step for the improvement.

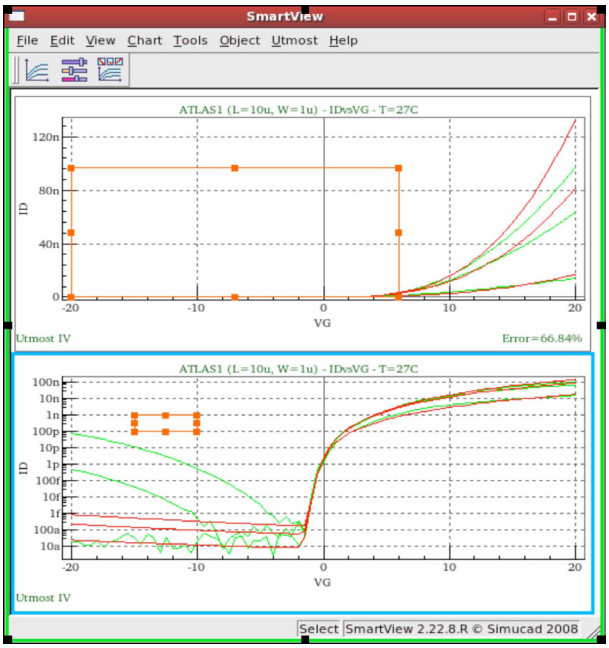

Figure 17: Utmost IV RPI a-Si TFT parameter optimization result: step 1.

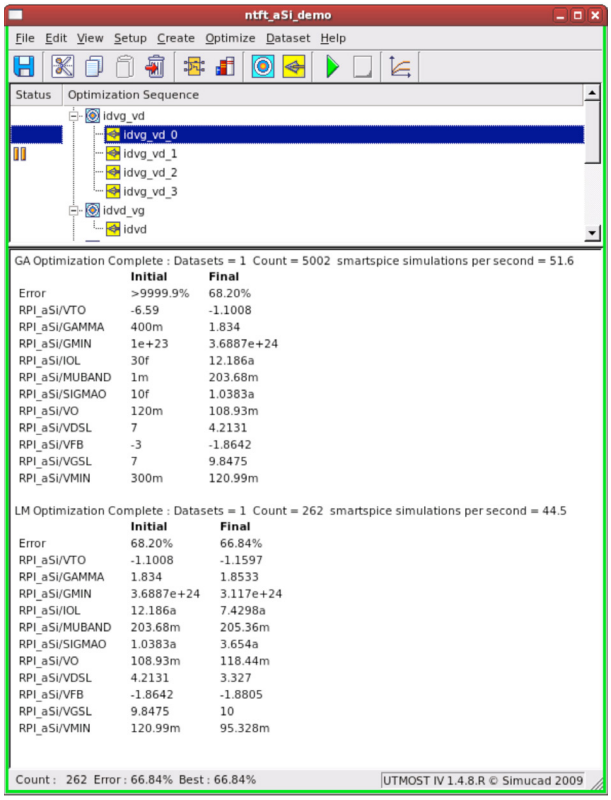

Figure 18: Utmost IV RPI a-Si TFT model optimization status: step 1.

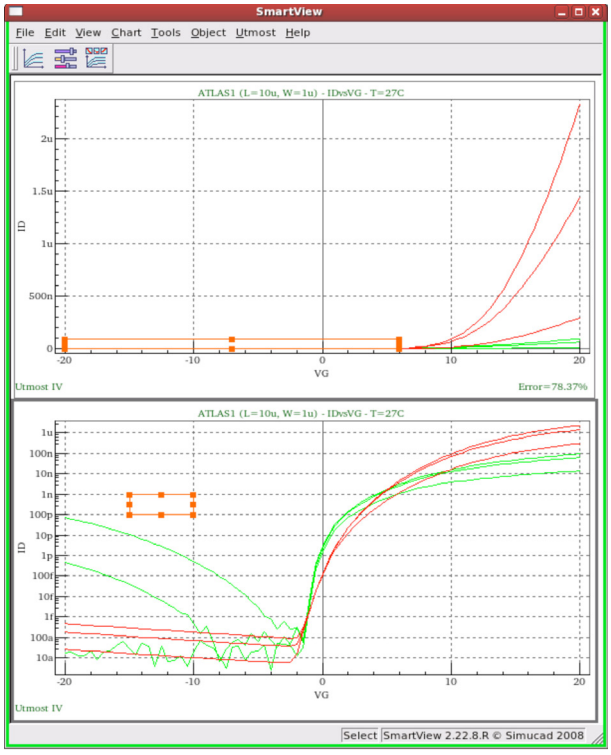

Figure 19: Utmost IV RPI a-Si TFT parameter optimization result: step 1 different result.

The first step result might be different from Figure 17 which looks like a Figure 19 as an example. The RPI a-Si TFT model user should accept it as the Utmost IV optimizer had to start the parameter optimization process using the completely unreasonable parameter values. Even though the step 1 result is unsatisfactory, the subsequent Utmost IV optimization sequence could find an adequate solution. The point is whether such characteristics as the drain leakage current at the negative Vgs, the sub-threshold, and the strong inversion regions are expressed qualitatively, or not.

2-2. Utmost IV RPI a-Si TFT Model Parameter Optimization: Step 2

The next step is to use both the sub-threshold and the saturation current regions as the optimization targets. It is shown as in Figure 20 which corresponds to Figure 17. The Figure 19 case in which the sub-threshold region is a little bit away from the target will be improved with this step as the optimization area of the sub-threshold region has the larger weight than for the linear scale area.

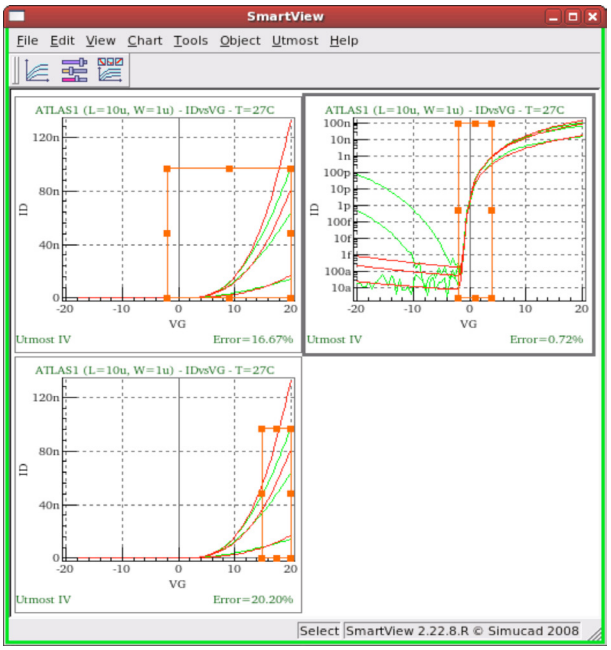

Figure 20: Utmost IV RPI a-Si TFT parameter optimization setup: step 2.

Figures 21 and 22 are for the step 2 result and the optimization status, respectively. The sub-threshold region keeps a good fitting, while the linear scale curves are improved.

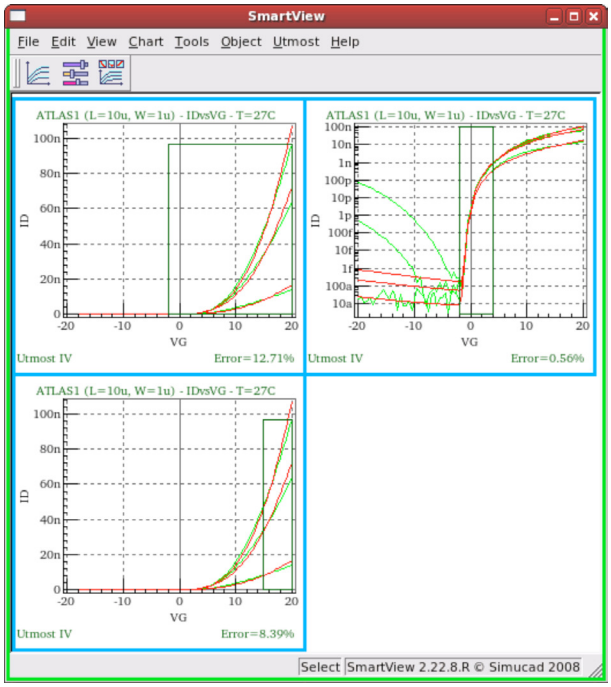

Figure 21: Utmost IV RPI a-Si TFT parameter optimization result: step 2.

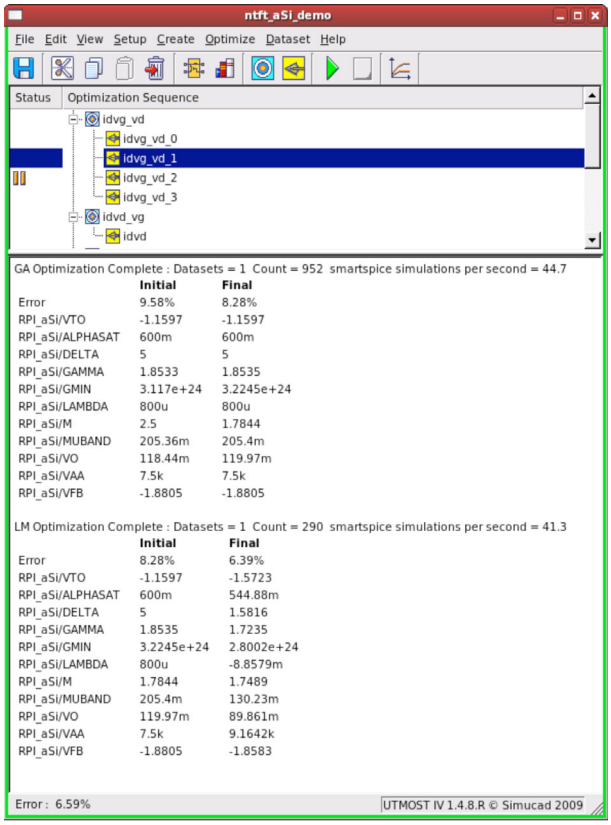

Figure 22: Utmost IV optimization status for step 2.

2-3. Utmost IV RPI a-Si TFT Model Parameter Optimization: Step 3

The next step is to optimize the negative Vgs drain leakage current region. This step could be right after the first step. The leakage current at the lowest Vds shows a different characteristic in this example data which is dropped from the optimization target. This is shown in Figure 23 in which Utmost IV plotted two Ids versus Vgs curves.

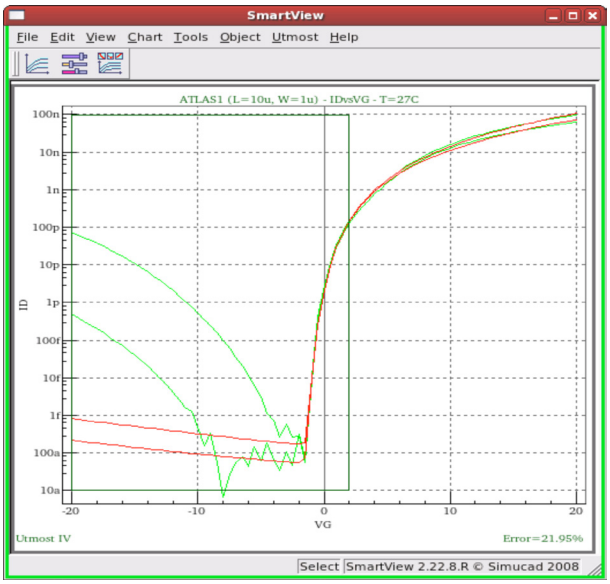

Figure 23: Utmost IV RPI a-Si TFT optimization set up: step 3.

Figures 24 and 25 are the step 3 result and the optimization status, respectively. Utmost IV hybrid optimizer succeeded in fitting the negative slope region of the drain current.

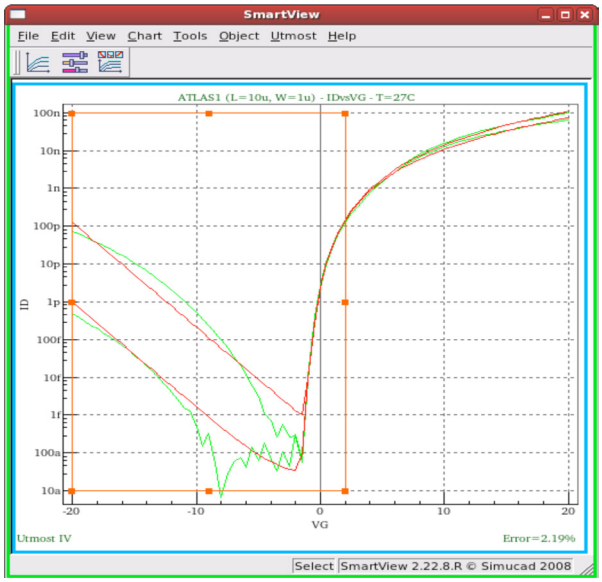

Figure 24: Utmost IV RPI a-Si TFT model parameter optimization result: step 3. The negative slope region of the drain current is expressed well.

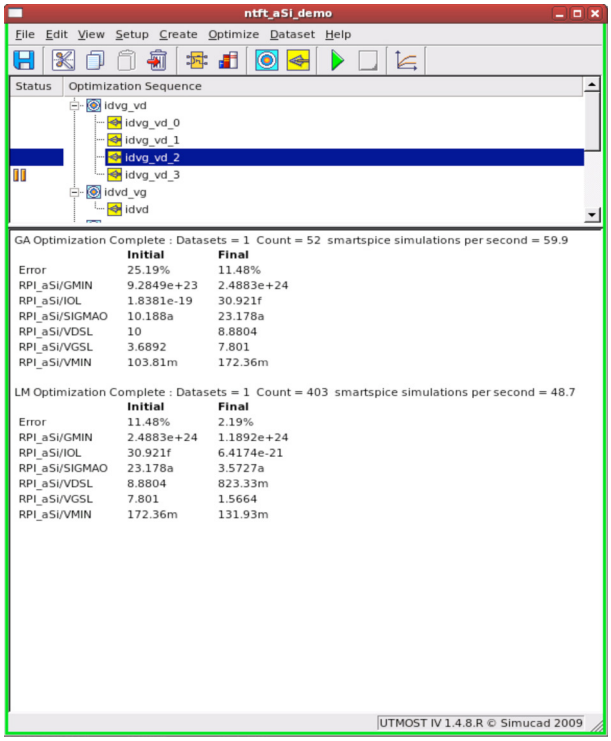

Figure 25: Utmost IV RPI a-Si TFT optimization status for step 3.

2-4. Utmost IV RPI a-Si TFT model parameter optimization: step 4

The next step is to balance the linear scale Ids versus Vgs and the sub-threshold region. Figure 26 shows the optimization target. The linear scale target region includes the sub-threshold current region to keep the region fitting in addition to the logarithmic scale target.

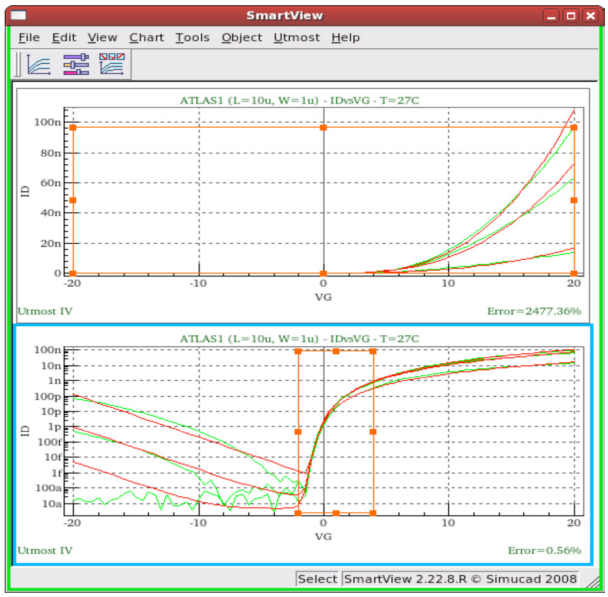

Figure 26: Utmost IV RPI a-Si TFT model optimization set up: step 4.

Figures 27 and 28 show the optimization result and the status, respectively.

Unfortunately, no improvement is observed for the liner scale data set.

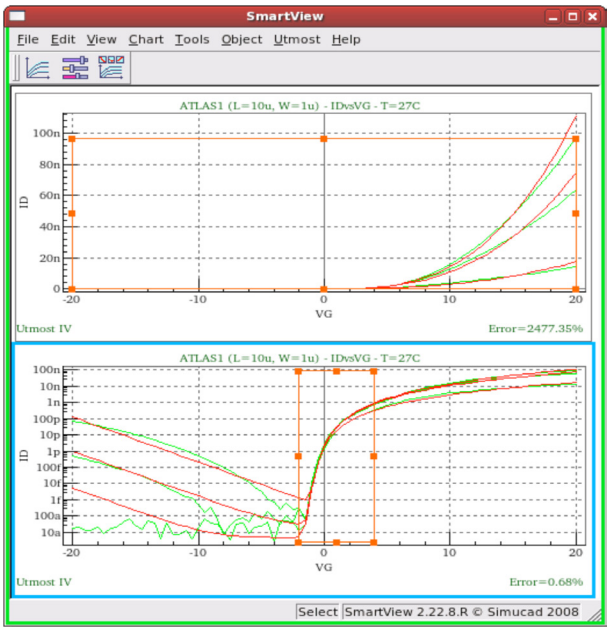

Figure 27: Utmost IV RPI a-Si TFT model optimization: step 4 result.

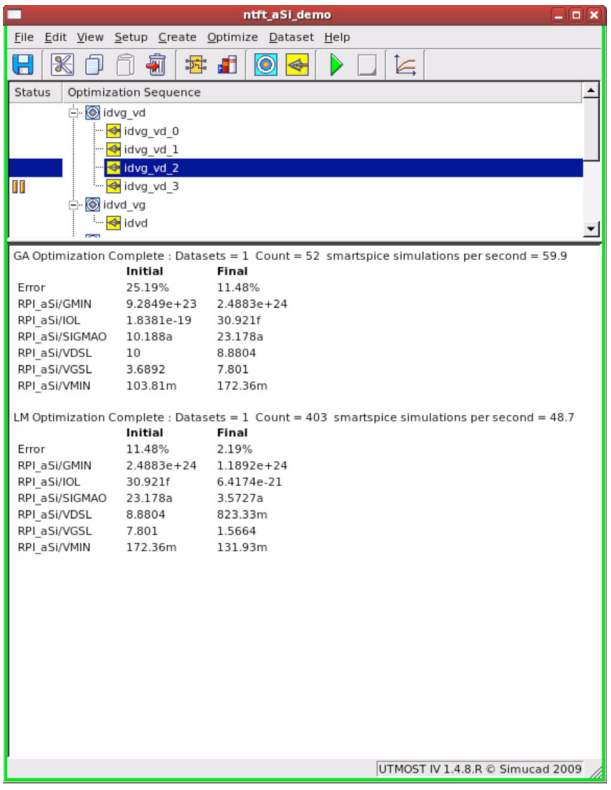

Figure 28: Utmost IV optimization status for step 4.

2-5. Utmost IV RPI a-Si TFT model parameter optimization: Step 5

The final step of the optimization sequence is to use the Ids versus Vds curves which are shown in Figure 29.

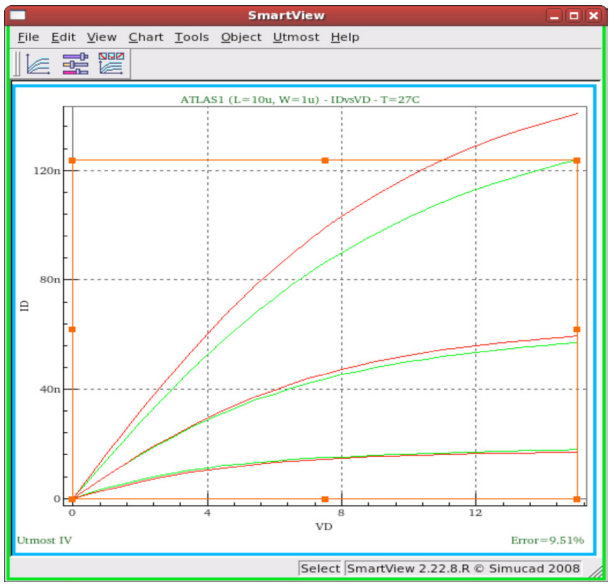

Figure 29: Utmost IV RPI a-Si TFT model optimization set up: step 5.

The previous steps using the Ids versus Vgs provided the good fitting as the initial value for the Ids versus Vds optimization. Figures 30 and 31 show the optimization result and the status, respectively. The simulation curves are very close to the target curves as in Figure 30. Utmost IV hybrid optimizer of the genetic algorithm and the Levenberg Marquardt method improved the fitting error.

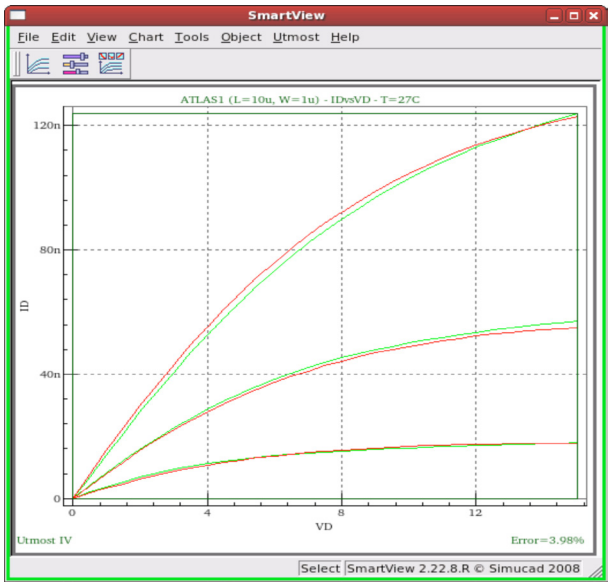

Figure 30: Utmost IV RPI a-Si TFT model optimization result: step 5.

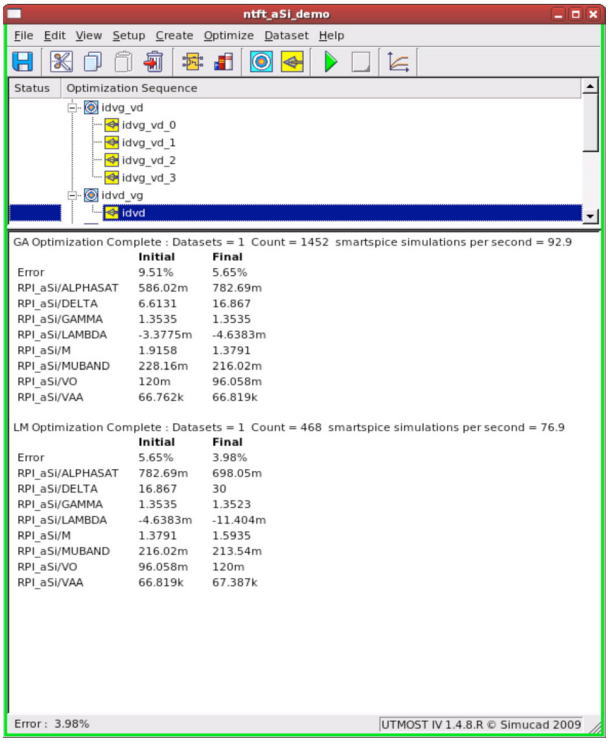

Figure 31: Utmost IV optimization status for step 5.

Although the Ids versus Vds curves are expressed well, the sub-threshold region has to be checked. It might be like in Figure 32 which shows that the sub-threshold is more degraded than in the previous step.

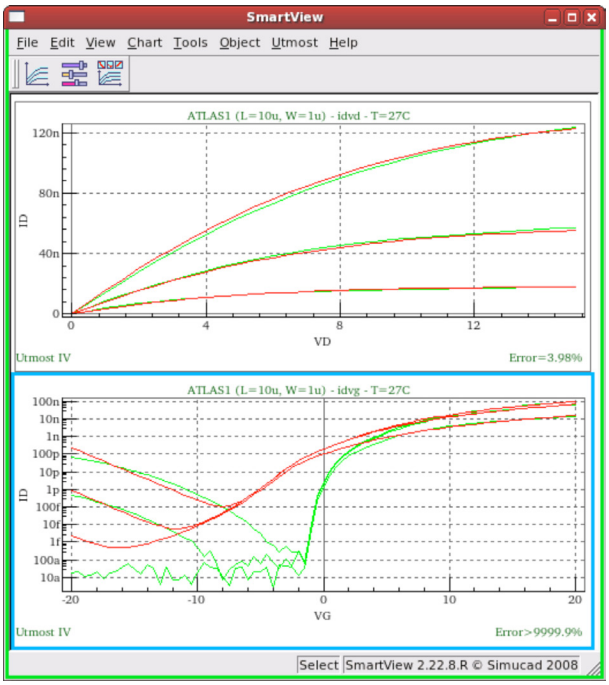

Figure 32: UTMOST IV RPI a-Si step 5 optimization result showing the sub-threshold degradation.

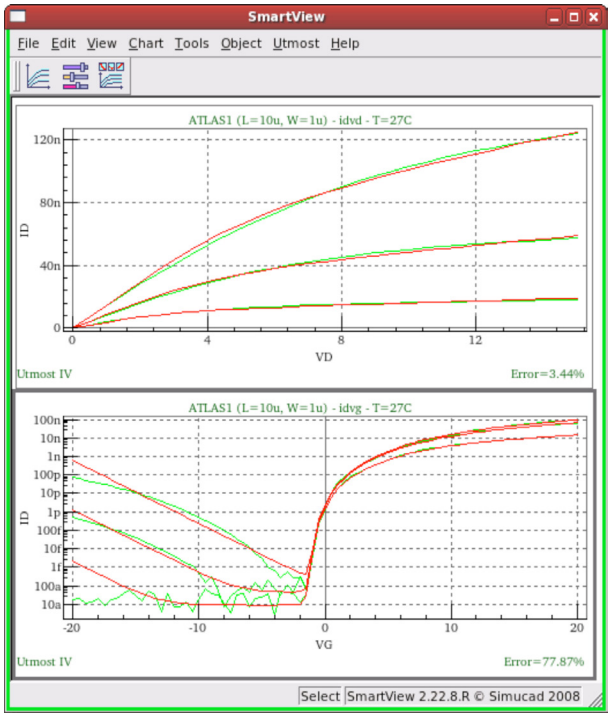

Figure 33: Utmost IV RPI a-Si TFT model optimization result: the same optimization sequence was repeated.

The improved result will be obtained by repeating the same optimization sequence. Figure 33 shows very good fitting for both the Ids versus Vds and the sub-threshold region. The fit error for the Ids versus Vds curves was 3.44%.

Numbers Regarding the Productivity and the Model Fitting

Utmost IV optimizer iterations were counted totally as 8,464 and 9,708 for the RPI poly-Si and a-Si TFT model examples, respectively. The required times for both sequences were less than four minutes using Intel Core 2 Duo machine with Red Hat Linux Enterprise-4. The fit errors of the Ids versus Vds curves for the RPI poly-Si TFT example were 16.4 % and 7.9 % for the L = 5 um and 8 um devices, respectively. The RPI a-Si TFT example showed the fit error of 3.44 %.

Conclusion

Silvaco Utmost IV hybrid optimizer demonstrated good productivity and the model fitting capability for both RPI poly-Si and a-Si TFT models.

TFT modeling engineers and SmartSpice simulator users can utilize the RPI TFT models more than ever.

References

[1] Silvaco LEARN TCAD with hundreds of examples tftex05.in: Forward/Reverse Gate Voltage Characteristic

http://www.silvaco.com/products/presentation/tcad/examples/tft/tftex05.html